

What is Claimed is:

1        1. In a timing trace stream having a logic signal  
2 associated with each clock cycle, the timing trace stream  
3 being transmitted in packets groups having a plurality of  
4 packets, a method of compressing the timing trace stream,  
5 the method comprising:

6        when each of a preselected number of clock cycles have  
7 at least one logic "1" signal and at least one logic "0"  
8 signal associated with each clock cycle, transmitting a  
9 standard group of packets having a logic signal associated  
10 with each of the preselected number of clock cycles; and

11        when the preselected number of clock cycles has only  
12 one of the logic "1" and the logic "0" signals associated  
13 with each clock cycle, transmitting a compressed group of  
14 packets, the packets including an indicia of the one logic  
15 signal, the packets including a signal group representing  
16 the preselected number.

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18        2. The method as recited in claim 1 wherein each  
19 group of packets has at least one header packet and at  
20 least one information packet.

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22        3. The method as recited in claim 2 wherein the  
23 standard group of packets includes a plurality of  
24 information packets and the compressed group of packets  
25 includes one information packet.

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2       4.    The method as recited in claim 1 further  
3            comprising:

4    representing an activity of the program counter with a  
5    first logic signal during a clock cycle; and

6        representing a non-activity of the program counter  
7    with a second logic signal during an associated clock  
8    cycle.

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10       5.   An apparatus for generating a timing trace stream  
11   in target processor, a logic signal being associated with  
12   each target processor clock cycle, the apparatus  
13   comprising:

14       a logic unit responsive to a preselected number of  
15   logic signals, the logic unit providing a first control  
16   signal when all of the preselected logic signals are  
17   different, the logic unit providing a second control signal  
18   when all of the preselected logic signals are the same;

19       a first storage unit responsive to the preselected  
20   logic signals for storing the each logic signal in a  
21   predetermined storage location, the first storage unit  
22   responsive to the first control signal for transferring the  
23   contents of the first storage unit; and

24       a second storage unit responsive to preselected logic  
25   signals for storing the current logic signal in a  
26   preestablished storage unit location, the second storage  
27   unit storing a signal group representing a multiple of the

1 preselected number, the second storage unit responsive to  
2 the second logic signal for transferring the contents of  
3 the second storage unit.

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5       6. The apparatus as recited in claim 5 wherein the  
6 storage location in the first and the second storage units  
7 are arranged in groups of packets, each group of packets  
8 including control signals with the packet payload.

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10       7. The apparatus as recited in claim 5 wherein each  
11 of the preselected number of logic signals represents an  
12 activity of the program counter during an associated clock  
13 cycle.

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15       8. The apparatus as recited in claim 5 further  
16 comprising a first in/first out storage unit, the contents  
17 of the first and the second storage unit being transferred  
18 to the first in/first out storage unit.

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20       9. A system for transferring data concerning the  
21 operation of target processor to a host processing unit,  
22 the system comprising:

23       a program counter trace stream generation unit, the  
24 program counter trace stream generation unit generating a  
25 trace stream identifying each activity of the program  
26 counter; and

1       a timing trace stream generation unit, the timing  
2 trace stream generation unit generating a timing trace  
3 stream with a logical signal each clock cycle, the logical  
4 signal identifying when the program counter performed an  
5 activity during the associated clock cycle, the timing  
6 trace stream including one type of signal group relating a  
7 logic signal with each of a predetermined number of clock  
8 cycles, the timing trace stream including a second type of  
9 signal groups identifying the predetermined number of clock  
10 cycles having the same logic signal.

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12       10. The system as recited in claim 9 wherein the  
13 trace streams include header packets and information  
14 packets.

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